REMARKS

Applicants appreciate the time taken by the Examiner to review Applicants' present application. This application has been carefully reviewed in light of the Official Action mailed February 9, 2005. Applicants respectfully request reconsideration and favorable action in this case.

DETAILED ACTION

The examiner stated that much of the claim terminology lacks antecedent basis. The Examiner stated:

> "In order to facilitate compact prosecution of the application, applicant's help is requested in correcting the following issues. Much of the claim terminology does not have proper antecedent basis in the specification as it relates to the specific embodiments. For example the examiner does not see in Figures 6a-c, 7a, 7b.or in the description of these Figures where the "first bit stream data clock" of at least claim 1 is identified. Note that at least claim 1 recites the phase detector of the pll as receiving the "first bit stream clock" and for example in Figure 6B the pll only receives the "REF CLK" signal. It is simply unclear whether the structure that generates the "REF_CLK" is the "first bit stream clock" of at least claim 1. This is due to the lack of proper antecedent basis. Similar situations exist with the other figures. Also the specification and drawings recite many different "Ref_clk" generators like 313,315, 326, 3405 344 and 346 that appear to not correspond to the circuit that produces the "Reference Clock Signal" of at least claim 1. It is simply unclear whether the structure that produces the "Reference Clock Signal" corresponds to the "first bit stream data clock" of at least claim 1 and it is unclear due to the lack of proper antecedent basis whether the many different "Ref_clk" generators like 313, 315, 326, 340, 344 and 346 correspond to structure that produces the "Reference Clock Signal" of at least claim 1. Also the terminology "phase detector to generate a phase

adjustment signal" which appears from the specification to be part of the Figure 6a embodiment is not shown. It is simply unclear what structure this corresponds to in the drawings. There are many other examples too numerious to mention specifically of the specification not providing proper antecedent basis for the claim terminology which makes the determination of what is being claimed difficult at best, thus in order to facilitate compact prosecution of the application, applicant's help is requested in correcting all these issues. On a related note, it appears that claims like claim 1 are linking claims, but due to the lack of proper antecedent basis an absolute determination cannot be made and thus the identification of what claims are linking claims below is done in so far as understood."

The applicant respectfully submits that Independent Claim 1 provides a high-speed bit stream data conversion circuit. When examining Figure 6A, we see a RX data demultiplexer circuit 308. This may correspond to the first data conversion circuit that here is receiving a single bit stream which may be at the nominal bit rate of 40 GBPS such as described with respect to Figure 5. The demultiplexer 308 produces four output bit streams by performing a 1 to 4 demultiplexing operation on the received single bit stream. These may vary between about 9.95 GBPS and 12.5 GBPS in one embodiment. RX data demultiplexer circuit 306 then receives these four bit streams and clock signals such as the QCLKI signal and TR_CLK clock signals from RX data demultiplexer circuit 308. RX data demultiplexer 306 performs a 1 to 4 demultiplexing operation to produce a total of 16 output bit streams from the four input bit streams.

The applicant respectfully submits that the first bit stream of Claim 1 is a bit stream defined by a first bit rate and corresponding first bit stream data clock (i.e. the first bit stream was clocked to a first bit stream data clock). The input to the first data conversion circuit is the first bit stream. The first bit stream data clock is not a separate input. Rather, the first bit stream data clock was originally used to create the first bit stream and is thus contained within the first bit stream. For example, a first data conversion circuit (RX DEMUX 308 of FIGs. 6A, 7A and

7B, and TX DATA MUX CIRCUIT 302 of FIGs. 6B and 6C) receives at least one first bit stream. The first bit stream(s), wherein the first bit stream contains (was clocked to) the first bit stream data clock , may be used by the clock circuit to produce a reference clock signal, (i.e. QCLKI of FIGs. 6A, 7A and 7B used to latch the first bit stream(s).

Therefore, the applicant respectfully submits that the "REF_CLK" is not the first bit stream clock of at least Claim 1. Rather, the first bit stream data clock of Claim 1 is the clock contained within the at least one first bit stream. The clock circuit that produces a referenced clock signal such as the QDCLK clock signal produced by PLL 317 is then used in the second demultiplexing operation to latch the at least one first bit stream based on a number of inputs provided, such as the LOS, LOL, QCLKI, TR_CLK, and REF_CLK inputs to the clock circuit. The first bit stream data clock is recovered from the first bit data stream and is provided as an input to the clock circuit. The clock circuit then chooses which clock will be used to latch data from the inputs provided.

With respect to the examiner's assertion that a phase detector to generate a phase adjustment signal which appears from the specification to be part of Figure 6A is not shown. The applicant respectfully submits and refers to Paragraph 55 where PLL 317 monitors frequency deviation between QCLKI and other references to produce a phase adjustment signal. Therefore, the applicant respectfully submits that PLL 317 and the associated logic circuits serve as a phase detector. Additionally, element 336 of Figure 6B is a phase detector.

While Applicants believe no other fees are due with this transmission, if any fees are due, the Commissioner is hereby authorized to charge Deposit Account No. 50-2126 of Garlick, Harrison & Markison, LLP.

If the Examiner has any questions or comments, or if further clarification is required, it is requested that the Examiner contact the undersigned at the telephone number listed below. Please reference Attorney Docket No. BP2517.

Respectfully submitted,

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